CLAIMS

1. A high voltage differential amplifier, comprising:

an input differential pair of low voltage transistors having a pair of control terminals receiving a differential input signal with a common mode voltage, a pair of first current terminals, and a pair of second current terminals coupled together at an input bias node;

a sense differential pair of low voltage transistors having a pair of control terminals receiving said differential input signal, a pair of first current terminals coupled together at a first sense node, and a pair of second current terminals coupled together at a second sense node, said first and second sense nodes each following said common mode voltage;

a first high voltage transistor having a first current terminal coupled to said second sense node, and a control terminal and a second current terminal coupled together at an output bias node that follows said common mode voltage;

a second high voltage transistor having a control terminal coupled to said output bias node, a first current terminal that develops a cascade bias node that follows said common mode voltage, and a second current terminal referenced to a power supply terminal;

a low voltage bias transistor having a first current terminal coupled to said first sense node, and a control terminal and a second current terminal coupled together at said cascade bias node;

a cascaded pair of low voltage transistors, each having a first current terminal coupled to a corresponding one of said pair of second current terminals of said input differential pair, a control terminal coupled to said cascade bias node, and a second current terminal; and

an output pair of high voltage transistors, each having a control terminal coupled to said output bias node, a first current terminal coupled to a corresponding one of said pair of second current terminals of said cascaded pair, and a second current terminal providing a corresponding polarity of a differential output signal.

2. The high voltage amplifier of claim 1, further comprising a differential converter circuit that converts said differential output signal to a single-ended output signal.

3. The high voltage amplifier of claim 1, wherein said low voltage transistors each have a breakdown voltage, and wherein said input bias node, said pair of first current terminals of said input differential pair, said first and second sense nodes, said output bias node and said cascade bias node each follow said common mode voltage within said breakdown voltage.

4. The high voltage amplifier of claim 1, wherein said low voltage transistors comprise BiCMOS transistors.

5. The high voltage amplifier of claim 1, wherein said high voltage transistors comprise DMOS transistors.

6. The high voltage amplifier of claim 1, wherein said low voltage transistors of said input differential pair and said sense differential pair comprise NPN BiCMOS transistors, wherein said low voltage bias transistor and said low voltage transistors of said cascaded pair comprise PNP BiCMOS transistors, and wherein said high voltage transistors comprise P-channel DMOS transistors.

7. The high voltage amplifier of claim 1, wherein said low voltage transistors of said input differential pair and said sense differential pair comprise PNP BiCMOS transistors, wherein said low voltage bias transistor and said low voltage transistors of said cascaded pair comprise NPN BiCMOS transistors, and wherein said high voltage transistors comprise N-channel DMOS transistors.

8. The high voltage amplifier of claim 1, wherein said low voltage transistors are bipolar transistors, wherein said high voltage transistors are DMOS transistors, wherein said pair of first current terminals of said input differential pair and said first bias node follow said common mode voltage, wherein said input bias node, said second sense node, and said cascade bias node each follow said common mode voltage within a base-to-emitter voltage, and wherein said output bias node follows said common mode voltage within a base-to-emitter voltage plus a gate-to-source voltage.

9. The high voltage amplifier of claim 1, wherein said input bias node, said first sense node, said output bias node and said pair of first current terminals of said differential input pair are each coupled to a corresponding one of a plurality of bias current devices.

10. The high voltage amplifier of claim 9, wherein each of said plurality of bias current devices comprises a MOS transistor coupled in series with a DMOS transistor and referenced to a power rail.

11. A high voltage rail-to-rail differential amplifier referenced to a high voltage power supply including positive and a negative terminals, comprising:

a high side amplifier circuit operative up to the positive terminal of the power supply; and

a low side amplifier circuit operative down to the negative terminal of the power supply; and

wherein each said amplifier circuit comprises:

an input stage including an input differential pair of low voltage transistors having input terminals receiving a differential input signal with a common mode voltage, a common terminal and a pair of amplifier terminals;

a bias sense stage including a sense differential pair of low voltage transistors having input terminals receiving said differential input signal, and current terminals coupled to form first and second sense nodes that slide with said common mode voltage;

a pair of high voltage transistors forming an output bias stage having a first current terminal coupled to said second sense node, a diode-coupled terminal forming an output bias node that slides with said common mode voltage, and a second current terminal forming a cascade bias node that slides with said common mode voltage;

a low voltage bias transistor diode-coupled to said cascade bias node and having a current terminal coupled to said first sense node;

a cascade stage including a cascaded pair of low voltage transistors having current terminals coupled in cascade with said amplifier terminals of said input differential pair and control terminals coupled to said cascade bias node; and

an output stage including a pair of high voltage transistors having control terminals coupled to said output bias node and current terminals coupled in series with said cascade stage to provide a differential output signal.

12. The high voltage rail-to-rail differential amplifier of claim 11, wherein said low voltage transistors each have a breakdown voltage, and wherein said common terminal, said pair of amplifier terminals, said first and second sense nodes, said output bias node and said cascade bias node each slide with said common mode voltage within said breakdown voltage.

13. The high voltage rail-to-rail differential amplifier of claim 11, wherein said low voltage transistors comprise BiCMOS transistors.

14. The high voltage rail-to-rail differential amplifier of claim 11, wherein said high voltage transistors comprise DMOS transistors.

15. The high voltage rail-to-rail differential amplifier of claim 11, wherein said low voltage transistors of said input stage and said bias sense stage of said high side amplifier circuit and wherein said low voltage transistors of said cascade stage and said low voltage bias transistor of said low side amplifier circuit each comprise NPN BiCMOS transistors, wherein said low voltage transistors of said input stage and said bias sense stage of said low side amplifier circuit and wherein said low voltage transistors of said cascade stage and said low voltage bias transistor of said high side amplifier circuit each comprise PNP BiCMOS transistors, wherein said high voltage transistors of said high side amplifier circuit comprise P-channel DMOS transistors, and wherein said high voltage transistors of said low side amplifier circuit comprise N-channel DMOS transistors.

16. The high voltage rail-to-rail differential amplifier of claim 11, wherein said low voltage transistors are bipolar transistors, wherein said high voltage transistors are DMOS transistors, wherein said first bias node and said amplifier terminals each slide at approximately the same voltage as said common mode voltage, wherein said common terminal, said second sense node and said cascade bias node each slide relative to said common mode voltage within a base-to-emitter voltage, and wherein said output bias node slides relative to said common mode voltage within a base-to-emitter voltage plus a gate-to-source voltage.

17. The high voltage rail-to-rail differential amplifier of claim 11, wherein said common terminal and said pair of amplifier terminals of said input stage, said output bias node and said first sense node are each coupled to a corresponding one of a plurality of bias current devices.

18. The high voltage rail-to-rail differential amplifier of claim 17, wherein each of said plurality of bias current devices comprises a MOS transistor coupled in series with a DMOS transistor and referenced to a corresponding one of said positive and negative power terminals.

19. A hot plug device, comprising:

a connector including a positive and negative voltage pins;

an input reference circuit coupled to said positive and negative voltage pins and providing sense and reference terminals;

a pass device having a current terminal coupled to said sense terminal and having a control input; and

a differential amplifier having a differential input coupled to said sense and reference terminals and an output coupled to said control input of said pass device, said differential input developing a common mode voltage, said differential amplifier comprising:

an input differential pair of low voltage transistors having a pair of control terminals coupled to said differential input, a pair of first current terminals, and a pair of second current terminals coupled together at an input bias node;

a sense differential pair of low voltage transistors having a pair of control terminals coupled to said differential input signal, a pair of first current terminals coupled together at a first sense node, and a pair of second current terminals coupled together at a second sense node, said first and second sense nodes each following said common mode voltage;

a pair of high voltage transistors forming an output bias stage having a first current terminal coupled to said second sense node, a diode-coupled terminal forming an output bias node that follows said common mode voltage, and a second current terminal forming a cascade bias node that follows said common mode voltage;

a low voltage bias transistor having a first current terminal coupled to said first sense node, and a control terminal and a second current terminal coupled together at said cascade bias node;

a cascaded pair of low voltage transistors, each having a first current terminal coupled to a corresponding first current terminal of said input differential pair, a control terminal coupled to said cascade bias node, and a second current terminal;

an output pair of high voltage transistors, having a pair of control terminals coupled to said output bias node, a pair of first current terminals coupled to a corresponding one of said second current terminals of said cascaded pair, and a pair of second current terminals providing a differential output signal; and

a differential conversion circuit that converts said differential output signal to said differential amplifier output.

20. The hot plug device of claim 19, wherein said low voltage transistors comprise BiCMOS transistors and wherein said high voltage transistors comprise DMOS transistors.